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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,804	08/01/2003	Naoki Kubo	Q76384	1990
23373	7590	06/30/2005	EXAMINER	
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/631,804	KUBO, NAOKI
Examiner	Art Unit	
Alexander O. Williams	2826	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 11 April 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 9,10 and 18-24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 9,10 and 18-24 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a))

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

Serial Number: 10/631804 Attorney's Docket #: Q76384
Filing Date: 8/1/2003; claimed foreign priority to 8/2/2002

Applicant: Kubo

Examiner: Alexander Williams

Applicant's Response filed 4/11/05 has been acknowledged.

Claims 1-8 and 11-17 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9, 10, 18 and 20 to 24 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hasebe et al. (U.S. Patent # 6,744,135 B2).

Claims 9 and similar claim 24 Hasebe et al. (figures 1 to 45B) specifically figure 1 (g) and 4 show an IC package comprising: an IC chip 115; a substrate 105 including a conductive layer (104,109,102 shown in figure 1g, but can be any metal layer in the substrate area connected to 117); a heat-radiating mechanism (117 shown in figure 1g and 401,402 shown in figure 4) that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, wherein the heat-radiating mechanism comprises plural laterally adjacent heat sinks (401,402, see figure 4), and at least part of each heat sink is disposed directly below the IC chip, and wherein terminals (118, the ones directly above and connected to 117) of the IC chip and the heat-radiating mechanism are electrically connected, and the heat-radiating mechanism and the conductive layer of the substrate are electrically connected.

10. The IC package of claim 9, Hasebe et al. show wherein the plural heat sinks 401,402 are disposed so as to be separate from each other.
18. The connection structure of claim 9, Hasebe et al. show wherein the IC chip is fixed on the heat-radiating mechanism.
20. The connection structure of claim 9, Hasebe et al. show wherein the IC chip and the heat radiating mechanism are electrically connected by a conductive material 118.
21. Hasebe et al. further show an insulating layer 111 between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members 116 disposed in plural through-holes 107 disposed in the insulating layer.
22. Hasebe et al. show the conductor layer is a ground layer (within the substrate but not labeled) and another conductor layer is a power layer.
23. Hasebe et al. further include an insulating layer 111 between the heat radiating mechanism 30 and the conductor layers 104 of the substrate, wherein said first of said plural heat sinks (401 in figure 4) and the ground layer are electrically connected via a first set of connection members disposed in plural through holes disposed in insulating layer, and wherein said second of said plural members disposed in plural through holes disposed in insulating layer.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of heat sinks and a conductor layer deals with an issue (i.e., the integration of multiple pieces into one

piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 9, 10 and 18 to 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (U.S. Patent Application Publication # 2003/0164549 A1).

Ion claims 9 and 24, Nakayama (figures 1 to 25) specifically figure 15 show an IC package comprising: an IC chip 20; a substrate 11 including a conductive layer (**a lower portion of 14**); a heat-radiating mechanism (**upper portion of 14**) that is mounted on the substrate, disposed between the IC chip and the substrate, and dissipates heat of the IC chip, wherein the heat-radiating mechanism comprises plural heat sinks (**upper portion of 14**), and at least part of each heat sink is disposed below the IC chip, and wherein terminals of the IC chip and the heat-radiating mechanism are electrically connected (**by 24**), and the heat-radiating mechanism and the conductive layer of the

substrate are electrically connected (**14 represent both, therefore, electrically connected**).

10. The IC package of claim 9, Nakayama show wherein the plural heat sinks **14** are disposed so as to be separate from each other.
18. The connection structure of claim 9, Nakayama show wherein the IC chip is fixed on the heat-radiating mechanism.
19. The connection structure of claim 9, Nakayama show wherein the IC chip and the heat-radiating mechanism are electrically connected by wire bonding **24**.
20. The connection structure of claim 9, Nakayama show wherein the IC chip and the heat radiating mechanism are electrically connected by a conductive material (**by 24**).
21. Nakayama further show an insulating layer (substrate material) between the heat-radiating mechanism and the conductive layer of the substrate, wherein the heat-radiating mechanism and the conductive layer of the substrate are electrically connected via connection members disposed in plural through-holes disposed in the insulating layer.
22. Nakayama show the conductor layer is a ground layer (within the substrate but not labeled) and another conductor layer is a power layer (within the substrate).
23. Nakayama further include an insulating layer (substrate material) between the heat radiating mechanism and the conductor layers of the substrate, wherein said first of said plural heat sinks **14** and the ground layer are electrically connected via a first set of connection members disposed in plural through holes disposed in insulating layer, and wherein said second of said plural members disposed in plural through holes disposed in insulating layer.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of heat sinks and the conductor layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Response

Applicant's arguments filed 4/11/05 have been fully considered, but are moot in view of the modified and new grounds of rejections detailed above. Applicant's arguments concerning Hasebe et al. have been considered and the rejection detailed above has been further detailed to describe the modified rejection above. Any metal element within the substrate area can be considered a conductive layer.

Field of Search	Date
U.S. Class and subclass: 257/684,796,666,698,696,675,784,786,692,693,691,712, 713,717,720	12/12/03 5/24/04 1/7/05 6/23/05
Other Documentation: foreign patents and literature in 257/684,796,666,698,696,675,784,786,692,693,691,712, 713,717,720	12/12/03 5/24/04 1/7/05 6/23/05
Electronic data base(s): U.S. Patents EAST	12/12/03 5/24/04 1/7/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
6/23/05



Primary Patent Examiner
Alexander O. Williams